REMARKS

Claims 1-7 and 56-59 were rejected under 35 U.S.C. §102(b) as being anticipated by Carollo, U.S. Patent 4,346,342. That rejection is respectfully traversed.

As discussed at page 25, with reference to Figure 22, most DC/DC converters incorporate a maximum current limit in their control circuitry. In particular, the current is limited such that it does not substantially exceed a maximum current I_{max}. In a fold back current limit approach, the current is reduced below I_{max} along a line 2203. Carollo similarly teaches such a fold back maximum current limiting approach. As illustrated in Fig. 2, the current follows the horizontal line at $V_{(reg)}$ to a maximum at point 64. Current is then held at that maximum between point 64 and point 65 and folds back from 65 to 67 and along 61. See column 5, lines 39-40 and 53-55, and column 6, lines 3 and 4.

Although a system embodying the present invention may include a maximum current limit as described, the present invention is directed to a novel minimum current limit which can avoid the problems associated with negative current flow in a DC/DC converter. As illustrated in Figure 22, current is limited at a minimum threshold I_{min}, which may be slightly negative. Similar to maximum current limits, the minimum current limit may be constant as illustrated at 2205, fold forward as illustrated at 2204 or fold back as illustrated at 2206.

Carollo teaches a maximum current limit comparable to the limit 2203 in Figure 22, but teaches nothing toward a minimum current limit as illustrated at 2204, 2205 and 2206. Thus Carollo fails to anticipate claims 1 and 56 and their dependent claims, each of which recites "a minimum current limit."

Claims 9-13 were rejected under 35 U.S.C. §103 as being unpatentable over Carollo in view of Goder, U.S. Patent 6,127,814. It is noted that there was no rejection of Claim 8, though it was not indicated to be allowable.

The rejection of Claims 9-13 is respectfully traversed. As discussed above, Carollo fails to suggest a minimum current limit. Goder, which was cited for use of a synchronous rectifier, also teaches nothing toward a minimum current limit; rather, it also deals with a maximum current limit (column 2, lines 20-23).

Claims 1 and 56 have been amended to parallel claims in a corresponding PCT application. In that application, U.S. Patent 3,824,450 was noted to effect a minimum current limit, but not with controlled rectifier transistors and for a very different purpose. Specifically, the present invention is directed to controlling amount of back drive current through a controlled rectifier transistor; whereas, the teachings of the '450 patent indicate that the rectifier 28 is a diode rectifier which would itself not allow back drive current. The '450 patent solves another problem not associated with controlled rectifiers, that of saturation of an internal controller when plural converters are placed in parallel. Since the rectifier 28 provided in the '450 patent is not able to conduct negative current, it is not possible to have a negative current flow through a controlled rectifier transistor (Claims 2 and 57) for a negative minimum current limit (Claims 12 and 77).

Thus, none of the cited references suggest a minimum current limit through a controlled rectifier transistor. Further, the references fail to teach a negative minimum current limit.

CONCLUSION

In view of the above amendments and remarks, it is believed that all claims are in condition for allowance, and it is respectfully requested that the application be passed to issue. If the Examiner feels that a telephone conference would expedite prosecution of this case, the Examiner is invited to call the undersigned at (978) 341-0036.

Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS, P.C.

By 

James M. Smith
Registration No. 28,043
Telephone: (978) 341-0036
Facsimile: (978) 341-0136

Concord, MA 01742-9133
Dated: 8/27/2

Claim Amendments Under 37 C.F.R. § 1.121(c)(1)(ii)

1. (Amended) A DC to DC power converter having an output comprising:

a controlled rectifier transistor through which the output current flows;

a control circuit which controls the output voltage; and

override control to the control circuit, responsive to a condition of the power converter or connected circuitry, to effect a minimum current limit of the output current flowing through the controlled rectifier transistor.

7. (Amended) A power converter as claimed in claim 5 wherein the signal indicative of output current is a [second] sensed current within the power converter.

56. (Amended) A method of converting DC to DC power comprising:

providing a controlled rectifier transistor through which output current flows;

controlling an output voltage through a control circuit; and

overriding control to the control circuit to effect a minimum current limit of the output current flowing through the controlled rectifier transistor.